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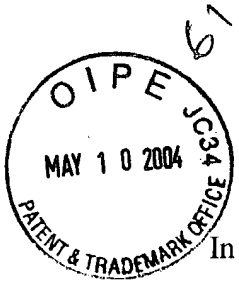

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

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In re application of

ROSHAN J. SAMUEL ET AL.

Serial No. 09/732,135 (TI-31249)

Filed December 7, 2000

For: PROGRAMMABLE STATE MACHINE INTERFACE

Art Unit 2181

Examiner Khanh Nmn Dang

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5-7-04

Jay M. Cantor, Reg. No. 19,906

BRIEF ON APPEAL

REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated, a Delaware corporation with offices at 7839 Churchill Way, Dallas, Texas 75251.

RELATED APPEALS AND INTERFERENCES

There are no known related appeals and/or interferences.

STATUS OF CLAIMS

This is an appeal of claims 1 to 3, 5 to 7 and 9 to 11, all of the rejected claims. No claims have been allowed. Please charge any costs to Deposit Account No. 20-0668.

STATUS OF AMENDMENTS

An amendment was not filed after final rejection.

SUMMARY OF INVENTION

The invention relates to a state machine input/output circuit responsive to a clock signal having cyclically repeating rising edges and falling edges for providing data to an output port. The machine, according to a first embodiment, includes a memory (300, 310, 320 of Fig 3) having a plurality of storage elements, each storage element being adapted to store a bit and provide the bit as an output of said memory. A first multiplexer (301, 311, 321) has a multiplexer output and a plurality of inputs receiving the outputs of the memory and has a control input (input from counter 33) for selecting, in response to a control signal (from control signal generator 33), an input for connection to the multiplexer output. A control signal generator (33) is connected to the control input of the first multiplexer for generating the control signal to control the first multiplexer to select the first multiplexer inputs for connection to the first multiplexer output. A clock edge selector circuit (306, 316, 326) is connected to the first multiplexer (via second multiplexer (305, 315, 325) and first and second flip-flops (302,303, 312,313, and 322,323) for providing , in response to an edge select signal from the clock edge selector circuit, the output of the multiplexer (301, 311, 321) to the output port selectably on either the rising edges or said falling edges of the clock signal.

The inputs of the first and second flip-flops are connected to the output of the first multiplexer, the first flip-flop changing states on the rising edge of a clock pulse and the second flip-flop changing states on the falling edge of a clock pulse. The outputs of the first and second flip-flops are connected to first and second inputs of the second multiplexer and the control input of the second multiplexer is connected to the output of the edge select register with the output of the second multiplexer being connected to the output port. A plurality of the input/output circuits can be provided for providing data to a plurality of output ports, the output ports being connected on an output data bus.

According to a second embodiment, the control registers and input multiplexers are eliminated for each output pin of the first embodiment and replaced with an additionl two-

input multiplexer 430, 440, 450 and flip-flop 431,441,451 configuration with one input of each input multiplexer being connected to a pin from the output data bus.

According to a third embodiment (Fig. 4), there is provided a memory 42 having a plurality of storage elements, each storage element being capable of storing a bit and providing the bit as an output of the memory. A first multiplexer 41 has an output, a plurality of inputs receiving the output of the memory and a control input for selecting, in response to a control signal, an input for connection to the output. A control signal generator 40 is connected to the first multiplexer for generating the control signal to control thed first multiplexer to select cyclically the first multplexer inputs for connection to the first multiplexer output. A second multiplexer (430, 440, 450) has a first input, a second input, an output, and a control input for selecting, in response to the control signal, an input for connection to the second multiplexer output. The first input is connected to a predetermined output data source, the output is connected to a data input of a first flip-flop (430, 440, 450) being clocked at the state machine clock rate. The second input is connected to an output of the first flip-flop and to the input of a clock edge selector circuit (436, 446, 456 et al.), and the control input is connected to the output of the first multiplexer. The clock edge selector circuit is connected to the second multiplexer for providing, in response to an edge select signal, the output of the second multiplexer to the output port selectably on either the rising edges or the falling edges of the clock signal. T inputs of the second and third flip-flops (432-433,442-443,452-453) are connected to the output of the second multiplexer, the second flip-flop (432, 442, 452) changing states on the rising edge of clock pulse and the third flip-flop (433, 443, 453) changing states on the falling edge of clock pulse. The outputs of the second and third flip-flops are connected to first and second inputs of a third multiplexer (435,445, 455) and the control input of the third multiplexer is connected to the output of the edge select register (436, 446, 456). The output of the third multiplexer is connected to the output port.

ISSUE

The issue on appeal is whether claims 1 to 3, 5 to 7 and 9 to 11 are anticipated by McCracken et al. (U.S. 6,279,073) under 35 U.S.C. 102(e).

GROUPING OF CLAIMS

The claims do not stand or fall together for reasons set forth hereinbelow under ARGUMENT.

ARGUMENT

Claims 1 to 3, 5 to 7 and 9 to 11 were rejected under 35 U.S.C. 102(e) as being anticipated by McCracken et al. The rejection is without merit as will be demonstrated.

It is basic that for a rejection under section 102 to be valid it is necessary that each and every element of a claim as well as each function of each element be shown in a single reference. This is not the case herein, contrary to the allegation of the Examiner.

Claim 1 requires, among other features, a memory having a plurality of storage elements, each storage element being adapted to store a bit and provide the bit as an output of the memory which the Examiner equates to DDR-SDRAM 16, 18 in Fig. 1 of McCracken et al. However, claim 1 further requires a first multiplexer having a multiplexer output, having a plurality of inputs receiving the outputs of said memory, and having a control input for selecting, in response to a control signal, an input for connection to the multiplexer output which the Examiner equates to "first multiplier (MUX) 104 having an output (116, Fig, 3, for example), having a plurality of inputs (See at least Fig. 1) receiving the outputs of the memory". It is clear that the multiplexer as claimed has *a plurality of input* whereas the multiplexer 104 of McCracken et al. not only does not have a plurality of bit inputs and does not have a plurality of inputs from the memory. It follows that McCracken et al. fails as a reference for this reason alone.

Claim 1 further requires a control signal generator connected to the control input of the first multiplexer for generating a control signal to control the first multiplexer to select the first multiplexer inputs for connection to the first multiplexer output.which the Examiner states is control signal 106 of McCracken et al. It is not seen how control signal 106 of McCracken et al. can be so equated when there is no data input from the memory to multiplexer 104 for selection in the first place.

Claim 1 yet further requires a clock edge selector circuit connected to the first multiplexer for providing , in response to an edge select signal, the output of the multiplexer to the output port selectably on either the rising edges or the falling edges of said clock signal. The Examiner apparently equates this feature with the circuit of Fig. 4 of McCracken et al. However, as can be seen in Fig. 4 of McCracken et al., there is no way of equating Fig. 4 of McCracken et al. to the claimed subject matter herein since Fig. 4 merely shows circuit elements the same or similar to those claimed, but not in the arrangement claimed. In fact, it is clear that though McCracken et al. may be used as a catalog for elements set forth in the claims herein, McCracken et al. is for an entirely different type of system, has an entirely different purpose and does not arrange the elements in the manner set forth in the claims either structurally or functionally.

Claims 2 and 3 depend from claim 1 and therefore define patentably over McCracken et al. for at least the reasons presented above with reference to claim 1.

In addition, claim 2 further limits claim 1 by requiring that the inputs of first and second flip-flops be connected to the output of the multiplexer, the first flip-flop changing states on the rising edge of clock pulse and the second flip-flop changing states on the falling edge of clock pulse. The Examiner equates the flip flops to latches 174 and 176 of McCracken et al. However, as can be seen, there is not connection from multiplexer 160 to latch 174.

Claim 2 further requires that the control input of the second multiplexer be connected to the output of an edge select register. No such structure is found in McCracken et al. connected to the second multiplexer 180 and multiplexer 188 is not connected to the outputs of both latches as required in the claim (assuming multiplexer 188 is equated with the second multiplexer).

The final rejection does not mention claim 3 and, accordingly, the propriety of the rejection cannot be reasonably argued.

Claim 5 requires, among other features, a clock edge selector circuit having an input connected to the input port and having an output, for selecting, in response to an edge select signal, data on the input port for provision to the selector circuit output selectably on either

the rising edges or the falling edges of the clock signal. No such structure is found in McCracken et al.

Claim 5 further requires a first multiplexer having a multiplexer output connected to a first flip-flop, the multiplexer having two inputs, a first one of the inputs receiving the selector circuit output, and a second one of the inputs connected to the output of the first flip-flop and to the sampled output port, and having a control input for selecting, in response to a control signal, the first input or the second input for connection to the first multiplexer output. No corresponding structure is found in McCracken et al. either alone or in the combination as claimed or has been shown by the Examiner to be present in McCracken et al.

Claim 5 still further requires a control signal generator connected to a second multiplexer for generating a control signal to control the second multiplexer to select the second multiplexer for connection to the second multiplexer output. No corresponding structure is found in McCracken et al. either alone or in the combination as claimed or has been shown by the Examiner to be present in McCracken et al.

Claim 5 yet further requires a memory having a plurality of storage elements, each storage element being adapted to store a bit and provide the bit at a memory output of the memory, the memory output being connected to the inputs of the second multiplexer, wherein the output of the second multiplexer selects the first input or the second input of the first multiplexer for connection to the first multiplexer output. No corresponding structure is found in McCracken et al. either alone or in the combination as claimed or has been shown by the Examiner to be present in McCracken et al.

Claims 6 and 7 depend from claim 5 and therefore define patentably over McCracken et al. for at least the reasons presented above with reference to claim 5.

In addition, claim 6 further limits claim 5 by requiring an input to the clock edge selector circuit connected to the input of a second and a third flip-flop being clocked at the state machine clock rate, the second flip-flop changing states on the rising edge of clock and the third flip-flop changing states on the falling edge of clock. No corresponding structure is found in McCracken et al. either alone or in the combination as claimed or has been shown by the Examiner to be present in McCracken et al.

Claim 6 still further requires that the outputs of the second and third flip-flops be connected to first and second input of a third multiplexer. No corresponding structure is found in McCracken et al. either alone or in the combination as claimed or has been shown by the Examiner to be present in McCracken et al.

Claim 6 yet further requires that the control input of the third multiplexer be connected to the output of an edge select register. No corresponding structure is found in McCracken et al. either alone or in the combination as claimed or has been shown by the Examiner to be present in McCracken et al.

Claim 6 even further requires that the output of the third multiplexer be connected to the output of the clock edge selector circuit. No corresponding structure is found in McCracken et al. either alone or in the combination as claimed or has been shown by the Examiner to be present in McCracken et al.

Claim 7 further limits claim 5 by requiring a plurality of the input/output circuits for passing data from an input port to a sampled output port, the input port being connected to an input data bus and the sampled output port being connected to an output bus. No corresponding structure is found in McCracken et al. either alone or in the combination as claimed or has been shown by the Examiner to be present in McCracken et al.

Claim 9 requires, among other features, a first multiplexer having an output, having a plurality of inputs receiving the output of said memory, and having a control input for selecting, in response to a control signal, an input for connection to said output. No corresponding structure is found in McCracken et al. either alone or in the combination as claimed or has been shown by the Examiner to be present in McCracken et al. at least for reasons as discussed in connection with claim 1.

Claim 9 further requires a control signal generator connecter to the first multiplexer for generating a control signal to control the first multiplexer to select cyclically the first multplexer inputs for connection to the first multiplexer output. No corresponding structure is found in McCracken et al. either alone or in the combination as claimed or has been shown by the Examiner to be present in McCracken et al.

Claim 9 further requires a second multiplexer having a first input and a second input, having an output, and having a control input for selecting, in response to a control signal, an input for connection to the second multiplexer output, the first input being connected to a predetermined output data source, the output being connected to a data input of a first flip-flop being clocked at the state machine clock rate, the second input being connected to an output of the first flip-flop and to the input of a clock edge selector circuit, and the control input being connected to the output of the first multiplexer. No corresponding structure is found in McCracken et al. either alone or in the combination as claimed or has been shown by the Examiner to be present in McCracken et al.

Claim 9 still further requires that the clock edge selector circuit be connected to the second multiplexer for providing, in response to an edge select signal, the output of the second multiplexer to the output port selectably on either the rising edges or the falling edges of the clock signal. No corresponding structure is found in McCracken et al. either alone or in the combination as claimed or has been shown by the Examiner to be present in McCracken et al.

Claims 10 and 11 depend from claim 9 and therefore define patentably over McCracken et al. for at least the reasons presented above with reference to claim 9.

In addition, claim 10 further limits claim 9 by requiring that the inputs of the second and third flip-flops be connected to the output of the second multiplexer, the second flip-flop changing states on the rising edge of clock pulse and the third flip-flop changing states on the falling edge of clock pulse. No corresponding structure is found in McCracken et al. either alone or in the combination as claimed or has been shown by the Examiner to be present in McCracken et al.

Claim 10 still further limits claim 9 by requiring that the outputs of the second and third flip-flops be connected to first and second inputs of a third multiplexer. No corresponding structure is found in McCracken et al. either alone or in the combination as claimed or has been shown by the Examiner to be present in McCracken et al.

Claim 10 yet further limits claim 9 by requiring that the control input of the third multiplexer be connected to the output of an edge select register. No corresponding

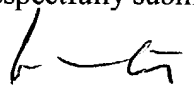
structure is found in McCracken et al. either alone or in the combination as claimed or has been shown by the Examiner to be present in McCracken et al.

Claim 11 further limits claim 9 by requiring a plurality of the input/output circuits for passing output data to an output port, the output port being connected to an output bus. No corresponding structure is found in McCracken et al. either alone or in the combination as claimed or has been shown by the Examiner to be present in McCracken et al..

CONCLUSIONS

For the reasons stated above, reversal of the final rejection and allowance of the claims on appeal is requested that justice be done in the premises.

Respectfully submitted,



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APPENDIX

The claims on appeal read as follows:

1. A state machine input/output circuit responsive to a clock signal having cyclically repeating rising edges and falling edges, for providing data to an output port, comprising:

a memory having a plurality of storage elements, each storage element being adapted to store a bit and provide the bit as an output of said memory;

a first multiplexer having a multiplexer output, having a plurality of inputs receiving the outputs of said memory, and having a control input for selecting, in response to a control signal, an input for connection to said multiplexer output;

a control signal generator connected to the control input of the first multiplexer for generating a control signal to control said first multiplexer to select said first multiplexer inputs for connection to said first multiplexer output; and

a clock edge selector circuit connected to said first multiplexer for providing , in response to an edge select signal, the output of said multiplexer to said output port selectably on either said rising edges or said falling edges of said clock signal.

2. The state machine input/output circuit of Claim 1, wherein said clock edge selector circuit, wherein:

the inputs of the first and second flip-flops are connected to the output of said multiplexer, said first flip-flop changing states on said rising edge of clock pulse and said second flip-flop changing states on said falling edge of clock pulse;

the outputs of said first and second flip-flops are connected to first and second inputs of a second multiplexer;

the control input of said second multiplexer is connected to the output of an edge select register; and

the output of said second multiplexer is connected to said output port.

3. The state machine input/output circuit of Claim 1, further comprising a plurality of said input/output circuits, for providing data to a plurality of output ports, wherein said output ports are connected on an output data bus.

5. A state machine input/output circuit responsive to a clock signal having cyclically repeating rising edges and falling edges, for passing data from an input port to a sampled output port, comprising:

a clock edge selector circuit having an input connected to said input port and having an output, for selecting, in response to an edge select signal, data on said input port for provision to said selector circuit output selectably on either said rising edges or said falling edges of said clock signal;

a first multiplexer having a multiplexer output connected to a first flip-flop, said multiplexer having two inputs, a first one of said inputs receiving said selector circuit output, and a second one of said inputs connected to the output of said first flip-flop and to the sampled output port, and having a control input for selecting, in response to a control signal, said first input or said second input for connection to said first multiplexer output;

a control signal generator connected to a second multiplexer for generating a control signal to control said second multiplexer to select said second multiplexer for connection to said second multiplexer output;

a memory having a plurality of storage elements, each storage element being adapted to store a bit and provide the bit at a memory output of said memory, said memory output being connected to the inputs of said second multiplexer, wherein the output of said second multiplexer selects said first input or said second input of said first multiplexer for connection to said first multiplexer output.

6. The state machine input/output circuit of Claim 6, wherein:

an input to said clock edge selector circuit is connected to the input of a second and a third flip-flop being clocked at said state machine clock rate, said second flip-flop changing states on said rising edge of clock and said third flip-flop changing states on said falling edge of clock;

the outputs of said second and third flip-flops are connected to first and second input of a third multiplexer;

the control input of said third multiplexer is connected to the output of a edge select register; and

the output of said third multiplexer is connected to said output of said clock edge selector circuit.

7. The state machine input/output circuit of Claim 5, further comprising a plurality of said input/output circuits, for passing data from an input port to a sampled output port, wherein said input port is connected to an input data bus and said sampled output port is connected to an output bus.

9. A state machine input/output circuit responsive to a clock signal having cyclically repeating rising edges and falling edges, for passing output data to an output port, comprising:

a memory having a plurality of storage elements, each storage element being capable of storing a bit and providing the bit as an output of said memory;

a first multiplexer having an output, having a plurality of inputs receiving the output of said memory, and having a control input for selecting, in response to a control signal, an input for connection to said output;

a control signal generator connected to said first multiplexer for generating a control signal to control said first multiplexer to select cyclically said first multplexer inputs for connection to said first multiplexer output;

a second multiplexer having a first input and a second input, having an output, and having a control input for selecting, in response to a control signal, an input for connection to said second multiplexer output, said first input being connected to a predetermined output data source, said output being connected to a data input of a first flip-flop being clocked at said state machine clock rate, said second input being connected to an output of said first flip-flop and to the input of a clock edge selector circuit, and said control input being connected to said output of said first multiplexer;

said clock edge selector circuit connected to said second multiplexer for providing, in response to an edge select signal, the output of said second multiplexer to said output port selectably on either said rising edges or said falling edges of said clock signal.

10. The state machine input/output circuit of Claim 9, wherein:

the inputs of said second and third flip-flops are connected to the output of said second multiplexer, said second flip-flop changing states on said rising edge of clock pulse and said third flip-flop changing states on said falling edge of clock pulse;

the outputs of said second and third flip-flops are connected to first and second inputs of a third multiplexer;

the control input of said third multiplexer is connected to the output of an edge select register; and

the output of said third multiplexer is connected to said output port.

11. The state machine input/output circuit of Claim 9, further comprising a plurality of said input/output circuits, for passing output data to an output port, wherein said output port is connected to an output bus.